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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/774,053	02/05/2004	Robert Steinfeld	P3223US1/APL1P300	4833

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EXAMINER	
CARPIO, IVAN HERNAN	
ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/774,053	STEINFELD ET AL.	
	Examiner	Art Unit	
	Ivan H. Carpio	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/27/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *26-31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18,20-23 and 25* is/are rejected.

7)☒ Claim(s) *19 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Examiner Note

Examiner acknowledges applicants election of group I, claims 1-25 without traverse for prosecution.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 8-11,13-18, 20-23 and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanahashi (US Patent 6184477).

With respect to claim 1 Tanahashi teaches an electrical mounting board (Fig. 2) comprising: a substrate having a plurality layers configured such that a substrate core (Fig. 2, element 13) lies between the layers; a first layer (Fig. 2, element G2) having formed thereon a plurality of bi-directionally oriented electrical ground traces arranged in a hybrid configuration so that a first group (Fig. 1, the vertical G2 traces) of electrical ground traces is arranged in a transverse relationship with a second group of electrical ground traces (Fig.1, the horizontal G2 traces), a second layer (Fig. 2, element G1) having formed thereon a plurality of bi-directionally oriented electrical ground traces arranged in a hybrid configuration so that a third group of electrical ground traces is arranged in a transverse relationship with a fourth group of electrical ground traces; a

set of electrically conductive interconnects (Fig. 2, element T_G) that pass through the substrate core to electrically connect electrical ground traces of the first layer with electrical ground traces of the second layer to form a multi-layer ground grid having a plurality of ringlets (Fig. 1), and signal traces formed (Fig.1, S1 or S2) between the electrical ground traces of at least one of the first and second layers.

With respect to claim 2, Tanahashi teach an electronic device (column 10, lines 35-37) incorporating the board of Claim 1.

With respect to claim 3 and with all limitations of claim 1, Tanahashi teaches that the electrical board comprises a two layer board (Fig. 2) wherein the first layer comprises a top layer of the board and wherein the second layer comprises a bottom layer of the board.

With respect to claim 4 and with all the limitations of claim 1 Tanahashi teaches that the electrical board comprises a board having at least three layers (Fig. 2).

With respect to claim 5 and with all the limitations of claim 1 Tanahashi teaches the electronic components (column 10, lines 35-37) are mounted on the board and electrically connected with the signal traces.

With respect to claim 6 and with all the limitations of claim 5, Tanahashi teaches that the electrical signal is provided to an electronic component (column 10, lines 35-37) using a signal trace; wherein the electronic component is electrically connected with an associated ringlet, and wherein the signal trace is configured so that it is positioned near the associated ringlet.

With respect to claim 8 and with all the limitations of claim 1, Tanahashi teaches that the plurality of electrical ground traces of the first layer overlay (Fig. 2) the plurality of electrical ground traces of the second layer to form a multi-layer grid having a plurality of ringlets configured such that the density (column 9,lines 1-6; since the grid line intervals can arbitrarily be selected, it would only make sense to select intervals that correspond to the number of components to be mounted) of the ringlets is related to the electrical components mounted on the board.

With respect to claim 9 and with all the limitations of claim 1, Tanahashi teaches that the ringlets are formed having different sizes (Fig. 1) at different areas of the board.

With respect to claim 10 Tanahasi teaches an electrical mounting board comprising: a substrate (Fig. 2) having a plurality layers configured such that a substrate core (Fig. 2, element 13) lies between the layers; a first layer (Fig. 2, element G2) having formed thereon a plurality of electrical ground traces configured in at least two groups arranged in a hybrid configuration so that a first group of substantially parallel electrical ground traces is arranged in a transverse relationship with a second group of substantially parallel electrical ground traces, a second layer (Fig. 2, element G1) having formed thereon a plurality of electrical ground traces configured in at least two groups arranged in a hybrid configuration so that a third group of substantially parallel electrical ground traces is arranged in a transverse relationship with a fourth group of substantially parallel electrical ground traces, a set of electrically conductive interconnects (Fig. 2, element T) that pass through the substrate core to electrically connect electrical ground traces of the first layer with electrical ground traces of the

second layer to form a multi-layer ground grid having a plurality of ringlets (Fig. 1); and signal traces formed on at least one of the first and second layers (Fig. 1, S1 or S2).

With respect to claim 11, Tanahashi teaches an electronic device incorporating the board of Claim 10.

With respect to claim 13 and with all the limitations of claim 10, Tanahashi that the electrical board comprises a two layer board (Fig. 2) wherein the first layer comprises a top layer of the board and wherein the second layer comprises a bottom layer of the board.

With respect to claim 14 and with all the limitations of claim 13 Tanahashi teaches that electronic components are mounted on at least one of the first and second layers (column 10, lines 35-37) and electrically connected with the signal traces and electrically grounded to the ground traces of the board.

With respect to claim 15 and with all the limitations of claim 14, Tanahashi teaches that the ringlets (Fig. 1 and Fig. 2) are located adjacent to the signal traces that electrically connect to the electronic components.

With respect to claim 16 and with all the limitations of claim 16, Tanahashi teaches that the electrical board comprises a multi-layer board (Fig. 2) having at least three layers.

With respect to claim 17 and with all the limitations of claim 10, Tanahashi teaches that the plurality of electrical ground traces of the first layer overlay the plurality of electrical ground traces of the second layer to form a multi-layer ground grid having a

plurality of ringlets configured in substantially square arrangements (Fig. 1 and Fig. 2, column 8 lines 66-67 and column 9 lines 1-6).

With respect to claim 18 and with all the limitations of claim 10, Tanahashi teaches that the plurality of electrical ground traces of the first layer overlay the plurality of electrical ground traces of the second layer to form a multi-layer ground grid having a plurality of ringlets configured in substantially diamond-shaped arrangements (Fig. 1 and Fig. 2, column 8 lines 66-67 and column 9 lines 1-6).

With respect to claim 20 and with all the limitations of claim 10, Tanahashi teaches that the plurality of electrical ground traces of the first layer overlay the plurality of electrical ground traces of the second layer to form a multi-layer ground grid having a plurality of ringlets configured such that the density of the ringlets is associated with the electrical components mounted with the board (Fig. 1 and Fig. 2, column 8 lines 66-67 and column 9 lines 1-6).

With respect to claim 21 and with all the limitations of claim 10, Tanahashi teaches that the signal traces are electrically connected with associated electronic components mounted on the board (column 10, lines 35-39).

With respect to claim 22 and with all the limitations of claim 21, Tanahasi teaches that the hybrid configurations of electrical ground traces on the first layer and the second layer are arranged to accommodate the arrangement of the signal traces and the associated electronic components that are mounted on the board (Fig.1 and Fig. 2).

With respect to claim 23 and with all the limitations of claim 22, Tanahasi teaches that the electronic components include electromagnetic field sensitive components

(column 10, lines 35-39) whose mode of operation is sensitive to variations in electromagnetic fields and wherein said plurality of ringlets are positioned underneath the electromagnetic field sensitive components to reduce the effects of undesirable electromagnetic emission.

With respect to claim 25 and with all the limitations of claim 10, Tanahashi teaches that the first layer is configured in at least three groups arranged in a hybrid configuration so that the first group (Fig. 1, the upper left half vertical ground traces) and the second group (Fig. 1, the upper right half horizontal ground traces) include a further fifth group (Fig. 1, the lower right half horizontal ground traces) comprising a plurality of substantially parallel electrical ground traces, wherein the first, second, and fifth groups are arranged so that each of said groups is in a transverse relationship with any adjacent group on the same layer, and wherein the second layer (Fig.1, same logic as above since they can have the same grid patter, column 8, lines 44-57) is configured in at least three groups arranged in a hybrid configuration so that the third group and the fourth group include a further sixth group comprising a plurality of substantially parallel electrical ground traces, wherein the third, fourth, and sixth groups are arranged so that each of said groups is in a transverse relationship with any adjacent group on the same layer.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanahashi.

With respect to claim 7 and with all the limitations of claim 6, Tanahashi teaches all of the limitations except does not specifically teach that the electrical current path defined by the signal trace and a return path through an associated ringlet is configured to minimize the loop area defined by the electrical current path. It is well known in the art that inductance is directly related to loop area and one would necessarily want to minimize the inductance and therefore the loop area. It would have been obvious to one of ordinary skill in the art at the time of the invention to configure the board in such a way to minimize the loop area, for the purpose of reducing unwanted inductance.

With respect to claim 12 and with all the limitations of claim 10, Tanahashi teaches all of the limitations except that the device is a computer. The use of multilayer circuit boards with ground grids and signal wiring in computers is well known. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the multilayer board, taught by Tanahashi, with a computer because of the of the high component mounting density and the uniformity of characteristic impedance offered by Tanahashi's circuit board prevents noise caused by reflection.

Allowable Subject Matter

The following is a statement of reasons for the indication of allowable subject matter: With respect to claim 19, there is simply no evidence in the prior art teaching or making obvious electrical ground traces of two layers forming ringlets configured in substantially triangular arrangements as in the claimed invention. With respect to claim 24, the prior art doesn't disclose a track pad positioned above a plurality of ringlets as in the claimed combination, furthermore there is no evidence in the prior art making obvious position a track pad above a plurality of ringlets as claimed.

Claims 19 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patents 5633479 and 4899439 both disclose similar ground grid arrays related to multi-layer circuit board.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ivan H. Carpio whose telephone number is 571-272-8396. The examiner can normally be reached on M-R 6:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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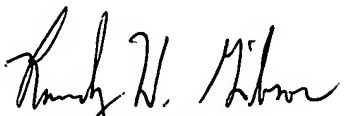

RANDY W. GIBSON
PRIMARY EXAMINER